Amendments to the Specification

Please replace paragraph [0031] starting at page 11, line 31 with the following amended version of that paragraph:

In FIG. 3 the XOR gate and associated circuitry (elements 350, ~~353,~~ 354, and 356) are pushed back one stage so that only a and b are affected by the additional logic delay. In a typical implementation, this stage of logic module 10' is implemented using single-ended NMOS pass transistors (like elements 354b-c and 356b-c), in contrast to the full CMOS MUX (like elements 254/258 in FIG. 2) used for the stages that process the c and d inputs. This means that the same number of pass transistors are required in FIGS. 2 and 3. In addition, the transistors in this stage can be smaller, so the total areas for the multiplexing is reduced. However, an extra inverter is required, which adds some area. Also an additional 2:1 MUX 30-3 is required to generate the p function for carry out multiplexer 70, which also adds area. Nevertheless, the area of the FIG. 3 embodiment can be approximately the same as the area of logic modules that do not implement arithmetic capabilities in the same way, and the present circuitry is more powerful (e.g., it can perform multiplication as well as addition). Note also that the c-to-logic-module-output speed of the FIG. 3 circuitry is greater because c does not go through any input multiplexer (as in some prior designs in which c is muxed with cin) before being input to the logic module.